

WHAT IS CLAIMED IS:

1. A differential amplifier, comprising:
a differential input capable of receiving a differential signal;
a first differential pair coupled to said differential input;
a second differential pair, coupled to said differential input, and
connected in parallel with said first differential pair at a differential output; and
a differential offset circuit, coupled between said differential input
and said second differential pair, and capable of level shifting said differential
signal from a first level to a second level.
2. The differential amplifier of claim 1, further comprising:
a differential switch circuit, coupled to said first differential pair
and said second differential pair, and capable of controlling a first current flow
to said first differential pair and a second current flow to said second differential
pair.
3. The differential amplifier of claim 1, wherein said differential
offset circuit comprises:
a first source follower coupled between a first input terminal of
said differential input and a first amplifying MOSFET of said second differential
pair; and
a second source follower coupled between a second input terminal
of said differential input and a second amplifying MOSFET of said second
differential pair.
4. The differential amplifier of claim 1, wherein said first differential
pair comprises a first MOSFET with a first drain terminal, and a second
MOSFET with a second drain terminal, and said second differential pair

Sub
A1

comprises a third MOSFET with a third drain terminal connected to said first drain terminal, and a fourth MOSFET with a fourth drain terminal connected to said second drain terminal.

5. A differential amplifier, comprising:
a differential input capable of receiving a differential signal;
a first differential pair coupled to said differential input;
a second differential pair, coupled to said differential input, and
connected in parallel with said first differential pair at a differential output; and
a differential switch circuit, coupled to said first differential pair
and said second differential pair, and capable of controlling a first current flow
to said first differential pair and a second current flow to said second differential
pair.

6. The differential amplifier of claim 5, further comprising:
a differential offset circuit, coupled between said differential input
and said second differential pair, and capable of level shifting said differential
input signal from a first level to a second level.

7. The differential amplifier of claim 5, wherein said differential
switch circuit comprises:
a first switch MOSFET coupled between said first differential pair
and a current source; and
a second switch MOSFET coupled between said second
differential pair and said current source.

8. A differential amplifier, comprising:
a differential input capable of receiving a differential input signal;
a first differential pair coupled to said first differential input, said

Sub
A1

10015887.121701

first differential pair biased with a first power supply voltage and a second power supply voltage;

a second differential pair, coupled to said differential input, and connected in parallel with said first differential pair at a differential output, said second differential pair biased with said first power supply voltage and said second power supply voltage; and

a differential switch circuit, coupled to said first differential pair and said second differential pair, and capable of controlling a first current flow to said first differential pair and a second current flow to said second differential pair.

9. The differential amplifier of claim 8, wherein said differential switch circuit changes said first current flow relative to said second current flow, based on a comparison between a common mode voltage of said differential input signal and a reference voltage.

10. The differential amplifier of claim 8, wherein said differential switch circuit increases said first current flow relative to said second current flow, when a common mode voltage of said differential input signal approaches said first power supply voltage.

11. The differential amplifier of claim 8, wherein said differential switch circuit decreases said first current flow relative to said second current flow, when a common mode voltage of said differential input signal approaches said second power supply voltage.

12. An amplifier, comprising:
an input capable of receiving an input signal;
a first amplifying MOSFET coupled to said input;

SLG
H

10015887 121701

Sub
H

a second amplifying MOSFET, coupled to said input, and connected in parallel with said first amplifying MOSFET at an output; and an offset circuit, coupled between said input and said second amplifying MOSFET, and capable of level shifting said input signal from a first level to a second level.

13. The amplifier of claim 12, wherein said offset circuit comprises: a source follower coupled between said input and said second amplifying MOSFET.

14. The amplifier of claim 13, wherein said source follower comprises:

a third MOSFET with a source terminal connected to a gate terminal of said second amplifying MOSFET; and

a fourth MOSFET with a drain terminal connected to said gate terminal.

15. The amplifier of claim 14, wherein said first amplifying MOSFET and said second amplifying MOSFET are a first type that is one of a NMOSFET and a PMOSFET.

16. The amplifier of claim 15, wherein said third MOSFET and said fourth MOSFET are a second type, said second type being opposite of said first type.

17. A method of extending an input signal range of a component that receives the input signal, comprising the steps of:

- (1) level shifting a voltage of the input signal; and
- (2) processing said level shifted voltage within the component.

18. The method of claim 17, wherein step (2) comprises the step of:
amplifying said level shifted voltage within the component.

19. The method of claim 17, further comprising the step of:
(3) selecting a subcomponent, from a plurality of
subcomponents within the component, to process said offset voltage.

20. The method of claim 19, wherein step (3) comprises the step of:
responding to a comparison between a common mode voltage of the input
signal and a reference voltage to select said subcomponent from said plurality of
subcomponents to process said offset voltage.

SCG
A1

10015887, 121701